TRENCH DMOS TRANSISTOR WITH EMBEDDED TRENCH SCHOTTKY RECTIFIER

STATEMENT OF RELATED APPLICATION

[0001] This case is related to application Ser. No. 09/684,931 filed Oct. 6, 2000 and entitled "Trench DMOS Transistor with Embedded Trench Schottky Rectifier".

FIELD OF THE INVENTION

[0002] The present invention relates to merged devices comprising power MOSFETs in parallel with Schottky barrier rectifiers. More particularly, the present invention relates to the merging of trench MOSFETs and trench Schottky w rectifiers into single devices, either on a single semiconductor substrate or as components in a larger integrated circuit.

BACKGROUND OF THE INVENTION

[0003] Power MOSFETs (metal oxide semiconductor field effect transistors) are well-known structures and are provided in a number of configurations, including the "vertical" DMOS transistor configuration illustrated in **FIG. 1** and the "trench" DMOS transistor configuration illustrated in **FIG. 2**. Each of the configurations shown includes a highly doped substrate **100** (shown as an N+region) on which is grown a lightly doped epitaxial layer **102** (shown as an N−region), which perform the drain function for the device. P-type body regions **104** (shown as P+/P and P−regions in **FIGS. 1 and 2**, respectively) are provided within the epitaxial layer **102**, as are source regions **112** (shown as N+regions). The device gates consist of conductive regions **111** and oxide regions **110**. A drain contact D is connected to the back surface of the semiconductor substrate **100**, a source and body contact SB is connected to the source regions **112** and body regions **104**, and a gate electrode G is connected to the conductive regions **111**. When a potential difference is applied across the body and the gate, charges are capacitively induced within the body region **104** adjacent to the gate oxide layer **110**, resulting in the formation of an N-type channel on the surface of the body region **104** adjacent to the gate of the DMOS cell. When another potential difference is applied across the source **112** and the drain **102,100**, carriers flow from the source to the drain through the channel as illustrated by the arrows in **FIGS. 1 and 2**, and the DMOS cell is said to be in a power-on state.

[0004] Power MOSFETs like those shown in **FIGS. 1 and 2** are often used in circuits that require a Schottky diode in parallel with the MOSFET. See, e.g., U.S. Pat. Nos. 4,823,172 and 6,049,108. Such a circuit configuration is shown schematically in **FIG. 3**. As can be seen from this figure, the low forward voltage drop of the Schottky diode **1** prevents the body-to-drain pn-junction diode **2** that is inherent in the DMOS structure from becoming forward biased when the source-to-drain voltage becomes positive. As a result, any current that does flow in the circuit of **FIG. 3** under these circumstances will flow through the Schottky diode.

[0005] By preventing the body-to-drain pn-junction diode from turning "on", the injection of minority carriers across the body-to-drain junction is prevented. If present, such minority carriers will delay a junction diode from turning "off" until all the carriers are either swept across the junction or they recombine after the voltage across the junction is reversed. The associated turn-off delay time limits the maximum frequency at which the MOSFET can operate.

[0006] On the other hand, the arrangement shown in **FIG. 3** allows essentially all of the current to flow through the Schottky diode. In contrast to the inherent body-to-drain pn-junction diode **2**, there is no turn-off delay associated with the Schottky diode **1**, because it is not a minority carrier device.

SUMMARY OF THE INVENTION

[0007] According to an embodiment of the invention, a merged device is provided, which comprises (1) a plurality of MOSFET cells that comprise: (a) a source region of first conductivity type formed within an upper portion of a semiconductor region, (b) a body region of second conductivity type formed within a middle portion of the semiconductor region, (c) a drain region of first conductivity type formed within a lower portion of the semiconductor region, and (d) a gate region provided adjacent the source region, the body region, and the drain region and (2) a plurality of Schottky diode cells disposed within a trench network, which Schottky diode cells comprise a conductor portion in Schottky rectifying contact with the lower portion of the semiconductor region. In this embodiment, at least one MOSFET cell gate region is positioned along a sidewall of the trench network and adjacent at least one Schottky diode cell.

[0008] According to another embodiment of the invention, a merged device is provided that comprises: (1) a semiconductor substrate of first conductivity type; (2) a semiconductor epitaxial layer disposed over the substrate; (3) a trench network extending into the epitaxial region from an upper surface of the epitaxial layer and forming a plurality of mesas within the device; (4) a plurality of MOSFET cells that comprise: (a) a source region of the first conductivity type disposed within one of the mesas, (b) a body region of second conductivity type disposed within the one of the mesas, wherein the body region forms a junction with the source region, (c) a drain region of first conductivity type at least partially disposed within the one of the mesas, wherein the drain region forms a junction with the body region; and (d) a gate region situated within the trench network such that it is adjacent the source region, the body region and the drain region, wherein the gate region comprises (i) an insulating region lining at least a portion of the trench network and (ii) a conductive region within the trench network adjacent the insulating region, the conductive region being separated from the source, body and drain regions by the insulating region; and (5) a plurality of Schottky dioide cells, which Schottky dioide cells are formed over bottom portions of the trench network and comprise a conductor portion that is in Schottky barrier rectifying contact with the epitaxial layer. The merged device of this embodiment is configured such that at least some of the MOSFET cell gate regions are positioned along sidewalls of the trench network adjacent the conductor portions of at least some of the Schottky diodes.

[0009] Certain preferred embodiments include one or more of the following characteristics: (a) the semiconductor is silicon, (b) the first conductivity type is n-type conductivity and the second conductivity type is p-type conductivity, (c) the gate region comprises a doped polysilicon region